Logic Analyzer Implemented on a FPGA Board

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Abstract

The aim of this work is a logic analyzer that records digital traces, displaying them on a monitor in VGA mode. The analyzer is implemented on a Spartan 2E XC2S200E FPGA board. User interface is provided through a PS2 keyboard that sends commands to the analyzer.

The main issue in realizing the display unit. The internal memory of the FPGA is too small to hold a full display memory of 640X480 pixels on 3 bits. The solution was found by realizing a character generator that displays characters corresponding to logic levels and their transitions. The screen is divided in a 64X48 character matrix

Start from the beginning moment of the acquisition, the acquiring unit buffers the data into a signal memory, at the moments of a signal change, and fills the 64X48X4 memory, with the character codes corresponding to the acquired logic levels at a specific moment. The user interface unit provides commands to the acquiring unit like

The logic analyzer presented above is a low-cost solution for displaying logic signals in educational laboratories.